UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,458	12/05/2003	Yi Song Chiu	N1085-90156	1305

8933 7590 09/21/2005

DUANE MORRIS, LLP
IP DEPARTMENT
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103-4196

EXAMINER	
DAHIMENE, MAHMOUD	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,458	CHIU ET AL.	
	Examiner	Art Unit	
	Mahmoud Dahimene	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/05/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~12/5/03~~ 3/3/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

10

DETAILED ACTION

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1,2,4,6,10 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Lim et al. (US 20050093063).

Lim et al. disclose a method for forming a multiple gate dielectric structure comprising the steps (Page 4, line 22) of; providing a first dielectric layer 14 (figure 1) overlying a substrate 12, forming a patterned photoresist overlaying the first dielectric layer, etching the exposed dielectric which reads on "removing second section of first insulator", perform photoresist removal to remove the masking layer and grow additional gate dielectric in at least one of multiple regions which reads on "performing a first photoresist removal procedure resulting in partial removal of said photoresist shape and forming a second insulator layer on said bare first section of said semiconductor substrate" (figure 7) (page 2, Paragraph 20), perform a post ash clean which reads on "performing a second photoresist removal procedure completely removing said photoresist shape", and oxidizing the dielectric layer causing the dielectric layer to have desired target thickness. Figure 6 shows a gate structure, with two gate insulator

thicknesses 42 and 54, and conductive layers 38 and 50 which reads on "performing a procedure to convert said first insulator layer located on a second section of said semiconductor substrate, to a first gate insulator layer, and to convert said second insulator layer to a second gate insulator layer, wherein the thickness of said first gate insulator is different than the thickness of said second gate insulator layer, and forming a first conductive gate structure on said first gate insulator layer and forming a second conductive gate structure on said second gate insulator layer".

As for applicants claims 2,10 and 11, Lim at al. disclose the dielectric layer could be silicon oxide (Page 4, claim 3) with a thickness between 30 and 70 Angstroms (Page 2, Paragraph 17) for the first oxide layer, and 20 Angstroms for the second oxide (Page 2, paragraph 20).

As for applicants claim 5, Lim at al. disclose a second dielectric (silicon dioxide) layer thickness is on the order or less than 10 Angstrom (Lim at al. claim 6)

As for applicants claim 6, Lim at al. cites the use of SPM for what they refer to as photoresist clean which reads on as a "second photoresist removal procedure" (Page 2, Paragraphs 20 and 21).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (US 20050093063) in view of Wolf et al. (Silicon Processing for the VLSI Era, Volume 1, Lattice Press, CA, 1986).

Applicants are claiming a method for forming a multi gate insulator layer where claim 3 consists of removing a section of an insulator layer, which could be silicon oxide, with a buffered hydrofluoric (BHF) solution.

Lim et al. disclose a similar method described above (section 2.) including a process step for etching a dielectric layer.

A difference is noted between applicant's claim and the reference of Lim.

Lim et al. fail to specify the method for said etch (Lim et al. claim 1).

Wolf et al. teach a common etch solution for silicon dioxide consisting of a buffered HF solution (Page 532) in conventional.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to select a buffered HF solution as the etchant in the process of Lim et al. to etch the first insulator layer, because a buffered HF solution maintains stable etch characteristics (Wolf et al.), and that it is conventional to include this step in semiconductor manufacturing process.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (US 20050093063) in view of Ryoo (US 6784060).

Applicants are claiming a method for forming a multi gate insulator layer where claim 4 consists of a first step for removing photoresist using ozone water.

Lim et al. disclose a similar method described above (section 2.) including an photoresist removal step (Lim et al., claim 1).

A difference is noted between applicant's claim 4 and the reference of Lim et al. Lim et al. fail to specify the exact photoresist removal procedure.

Ryoo discloses a similar semiconductor manufacturing process where the photoresist removal is performed with an ozone water solution (column 3, line 18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Lim et al. to include ozone water as the photoresist removing solution because it improves gate oxide reliability and oxidizes the exposed silicon surface as taught by Ryoo (column 6, line 59).

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (US 20050093063) in view of Shimizu et al. (US 20050158671 A1).

Applicants are claiming a method for forming a multi gate insulator layer where claim 7 consists of a photoresist removal procedure performed at temperatures between about 110°C and 150°C.

Lim et al. disclose a similar method described above (section 2.) including a process step for removing photoresist.

A difference is noted between applicant's claim 4 and the reference of Lim et al.

Lim et al. fail to specify a temperature range.

Shimizu et al. disclose a method for stripping photoresist, using SPM where the preferred temperature range is 100°C to 150°C (Page 4, paragraph 71).

Since Lim et al. do not restrict the temperature during photoresist removal, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to select a temperature of 110°C to 150°C in the process of Lim et al. Shimizu et al. illustrates that such a temperature range is effective for accomplishing photoresist removal. One of ordinary skill would be motivated to select such a temperature range because it is known to be effective to accomplish photoresist removal.

7. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (US 20050093063) in view of Wolf et al. (Silicon Processing for the VLSI Era, Volume 1, Lattice Press, CA, 1986).

Applicants are claiming a method for forming a multi gate insulator layer where claim 8 consists of using an oxygen-steam oxidation procedure, and claim 9 consists of performing the oxidation in a temperature range between 800 to 1050°C.

Lim et al. disclose a similar method described above (section 2.) including a process step for growing a thermal oxide layer.

A difference is noted between applicant's claims 8, 9 and the reference of Lim et al. Lim et al. fail to specify oxygen-steam ambient, and to specify a temperature range (Lim at al., claim19).

Wolf et al. teachings cite an oxygen-steam oxidation where the recommended temperature range is 800 to 1000°C (Page 215). Steam accelerates the oxidation process as compared to pure oxygen.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Lim et al. to use oxygen-steam for the oxidation process in a temperature range of 800 to 1000°C because as taught by Wolf, this is a conventional step in semiconductor manufacturing process.

8. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (US 20050093063) in view of Wolf et al. (Silicon Processing for the VLSI Era, Volume 2., Lattice Press, CA , 1990).

Applicants are claiming a method for forming a multi gate insulator layer where claims 12 and 13 consist of using doped polysilicon or a metal silicide as a conductive gate structure material.

Lim et al. disclose a similar method described above (section 2.) including a multi-gate structure with conductive gate electrode material (Lim at al., figure 6, items (38) and (50)).

It is noted that Lim et al. fail to specify the gate electrode material.

Wolf et al. cite doped polysilicon (Pages 318 and 398) and Tantalum silicide (Page 398) are commonly used as gate electrode materials.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Lim et al. to use doped polysilicon or Tantalum silicide as gate conductive materials because they are conventional gate electrode materials in semiconductor manufacturing process as taught by Wolf.

9. Claims 14,15,16,17,19, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (US 20050093063) in view of Ryoo (US 6784060).

Applicants are claiming a process of forming a semiconductor device comprising steps of, forming a first silicon oxide layer on entire surface of said semiconductor substrate of forming a photoresist shape on a first section of said first silicon oxide layer, in a region overlying a first section of said semiconductor substrate, removing second section of said first silicon oxide layer exposing a bare second section of said semiconductor substrate, performing an ozone containing mixture procedure to partially remove said photoresist shape and to form a second silicon oxide layer on said bare second section of said semiconductor substrate, performing a sulfuric acid - hydrogen peroxide mixture (SPM) procedure to completely remove said photoresist shape, performing an oxidation procedure to convert said first silicon oxide layer to a first gate insulator layer on said first section of said semiconductor substrate, and to convert said second silicon oxide layer to a second gate insulator layer, wherein the thickness of said

first gate insulator is greater than the thickness of said second gate insulator layer, forming a first conductive gate structure on said first gate insulator layer and forming second conductive gate structure on said second gate insulator layer.

Lim et al. disclose a process of forming a multi-gate dielectric structure for a semiconductor device which reads on "forming a semiconductor device" showing similar steps.

A difference is noted between applicant's claims and the reference of Lim et al. Lim et al. fail to specify "an ozone containing mixture procedure to partially remove photoresist" in the step corresponding to step (d) of applicant's claim 14.

Ryoo discloses a semiconductor manufacturing process for removing photoresist similar to step applicant's claim 14 where photoresist removal is performed with an ozone water solution (column 3, line 18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Lim et al. to include ozone water as the photoresist removing solution because it improves gate oxide reliability and oxidizes the exposed silicon surface as taught by Ryoo (column 6, line 59).

As for claim 15, Lim et al. describe a first silicon oxide thickness of 30 to 70 Angstroms (Page 3, paragraph 23).

As for claim 16 and 17, Lim et al. note that conventional etch processes may be used to remove portions of the dielectric (silicon oxide) layer (Page 2, paragraph 19). Also, BHF solutions and CHF3 plasmas are conventional etch processes for silicon oxide (See Wolf et al. Vol. 1, page 532, and page 581).

As for claim 19, Lim et al. cite a second oxide thickness in the range of 5 to 10 Angstroms (Page 2, paragraph 19).

As for claim 22, Lim et al. disclose a first silicon dioxide layer with a thickness between 30 and 70 Angstroms (Page 2, paragraph 17).

As for claim 23, Lim et al. disclose a second silicon dioxide layer with a thickness between 15 to 20 Angstroms (Page 2, paragraph 20).

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (US 20050093063) in view of Ryoo (US 6784060) and further in view of Yates et al. (US 20020173156 A1).

Applicants are claiming a process of forming a semiconductor device a process described above wherein claim 18 uses ozone water at 20 to 50°C for removing a photoresist layer.

Lim as modified by Ryoo has been described above in paragraph 9. Unlike the instant claimed invention as per claim 18, Lim and Ryoo fail to disclose performing the ozone water procedure at the specific temperature.

Yates et al. disclose a method for removing photoresist where an ozone water solution is used at 30°C (Page 3, paragraph 26) because ozone is more soluble in water at lower temperature.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Lim and Ryoo to include the

teachings of Yates to use ozone water at 30°C to obtain a high oxidation rate because ozone is more soluble in water at lower temperatures.

11. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (US 20050093063) in view of Ryoo (US 6784060) as applied to claims 14,15,16, 17,19, 22 and 23 and further in view of Shimizu et al. (US 20050158671 A1).

Applicants are claiming a method for forming a semiconductor device as described above, where claim 20 consists of a photoresist removal procedure performed at temperatures between about 110°C and 150°C.

Lim as modified by Ryoo disclose a similar method described above, including a process step for removing photoresist.

A difference is noted between applicant's claim 4 and the reference of Lim et al. modified by Ryoo, they fail to specify the temperature range for performing the procedure.

Shimizu et al. disclose a method for stripping photoresist, using SPM where the preferred temperature range is 100°C to 150°C (Page 4, paragraph 71).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Lim et al. to include a temperature range, for photoresist removal, between 110°C and 150°C because it is conventional to include this temperature range in the steps of semiconductor manufacturing process as taught by Shimizu.

12. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (US 20050093063) in view of Ryoo (US 6784060) and further in view of Wolf et al. (Silicon Processing for the VLSI Era, Volume 1., Lattice Press, CA , 1986).

Applicants are claiming a method for forming a semiconductor device as described above, where claim 21 consists of using an oxidation procedure in a temperature range between 800 to 1050°C.

Lim as modified by Ryoo disclose a similar method described above (section 2.) including a process step for growing a thermal oxide layer, but fail to specify a temperature range (Lim at al., claim19).

Wolf et al. teach an oxygen-steam oxidation where the recommended temperature range is 800 to 1000°C (Page 215). Steam accelerates the oxidation process as compared to pure oxygen.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Lim and Ryoo to use oxygen-steam for the oxidation process in a temperature range of 800 to 1050°C because it is a conventional step in semiconductor manufacturing process as taught by Wolf.

13. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (US 20050093063) in view of Ryoo (US 6784060) and further in view of Wolf et al. (Silicon Processing for the VLSI Era, Volume 2., Lattice Press, CA , 1990).

Applicants are claiming a method for forming a multi gate insulator layer where claims 12 and 13 consists of using doped polysilicon or a metal silicide as a conductive gate structure material.

Lim as modified by Ryoo disclose a similar method described above (section 2.) including a multi-gate structure with conductive gate electrode material (Lim at al., figure 6 items (38) and (50)). It is noted that Lim at al. fail to specify the gate electrode material.

Wolf et al. cite doped polysilicon (Pages 318 and 398) and Tantalum silicide (Page 398) are commonly used as gate electrode materials.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Lim and Ryoo to use doped polysilicon or Tantalum silicide as gate conductive materials because they are conventional gate electrode materials in semiconductor manufacturing process as taught by Wolf.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mahmoud Dahimene whose telephone number is (571) 272-2410. The examiner can normally be reached on week days from 8:00 AM. to 5:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MD

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER